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IN THE UNITED STATES PATENT & TRADEMARK OFFICE

IN RE APPLICATION OF	:
SHINICHI YOSHIOKA	: EXAMINER: FLORES, LEON
SERIAL NO: 10/798,403	:
FILED: MARCH 12, 2004	: GROUP ART UNIT: 2611
FOR: SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE AND METHOD OF TESTING THE SAME	:

AMENDMENT

COMMISSIONER FOR PATENTS
ALEXANDRIA, VIRGINIA 22313

SIR:

In response to the Office Action of April 24, 2007, please amend the above-identified application as follows:

Amendments to the Specification begin on page 2 of this paper.

Amendments to the Claims are reflected in the listing of claims which begins on page 4 of this paper.

Remarks begin on page 13 of this paper.

IN THE SPECIFICATION

Please replace the paragraph at page 3, lines 16-26, with the following rewritten paragraph:

In the known loop-back testing method, however, the clock source of the transmitter TX is the same as that of the receiver RX. Since the same clock source is used, there is no frequency offset between the clocks. The PI cannot properly activate itself if there is no frequency offset. For example, the PI keeps locking itself to a certain point in [[its]] the clock phase position diagram. Accordingly, testing concerning this PI remains unsatisfactory, so the fault coverage of the CDR circuit does not rise.

Please replace the heading at page 7, line 15, with the following rewritten heading:

BRIEF DESCRIPTION OF ~~THE SEVERAL VIEWS OF~~ THE ~~DRAWING~~ DRAWINGS

Please replace the paragraph beginning at page 17, line 9 to page 18, line 3, with the following rewritten paragraph:

A loop-back path is an electrical path for looping output serial data from the transmitter back to the receiver. In this embodiment, serial data is looped back crosswise between adjacent channels. For example, serial data transmitted from a first channel A-ch is looped back to a second channel B-ch. On the other hand, serial data transmitted from the second channel B-ch is looped back to the first channel A-ch. This loop-back path need only be formed at least either outside or inside the semiconductor integrated circuit device chip. In this embodiment, the loop-back path is formed inside the semiconductor integrated circuit device chip. The advantage of the loop-back path formed inside the chip is that the semiconductor integrated circuit device can be tested without the device [[is]] being connected to a testing substrate having a loop-back path. Therefore, the receiver can be

tested in the form of a wafer. For example, a plurality of devices can be simultaneously tested in the form of a wafer. Since this shortens the time required for the test, it is possible to, e.g., improve the throughput and shorten the TAT (Turn Around Time) of the product.

Please replace the paragraph beginning at page 24, line 22 to page 25, line 6, with the following rewritten paragraph:

In the third embodiment, unlike in the first and second embodiments, the length of a loop-back path from the first channel A-ch to the second channel B-ch differs from that of a loop-back path from the second channel B-ch to the first channel A-ch. If this difference between the loop-back path lengths can have a certain influence on testing, ~~it may be used~~ the arrangement pattern of the first and second embodiments can be used. If the length difference has no influence on testing, the arrangement pattern of the third embodiment can be used.

Please replace the paragraph at page 26, lines 6-10, with the following rewritten paragraph:

In the first to fourth embodiments, loop-back paths ~~for looping~~ loop back data to connect different channels such that these loop-back paths are connected in the form of a so-called "cross couple connection" between the different channels.